Quantum Computing: Realization of Quantum Hardware

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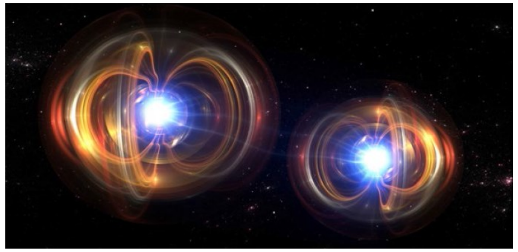
Advanced Radio IC Lab (ARIL)

Outline

- Motivation
- Quantum World: Key Concepts
- DiVincenzo Criteria for Computation
- Quantum Technologies Compared
- Fundamentals of Qubit Control
- Scaling Challenges
- State-of-the-art Cryogenic Controller IC
- Cryogenic controller IC challenges
- IIT Delhi controller chip design
- Summary

Motivation

- Quantum computers are exponentially faster in solving certain intractable problems
  - Security
    - Shor's algorithm, RSA encryption
  - Quantum chemistry
    - **Rapid vaccine development (e.g. Covid-19)**
    - Drug discovery
  - Optimization
    - Optimizing traffic route
  - Meteorology
    - Weather forecast



Jongseok, ISSCC 2021

Quantum World: Key Concepts

Superposition

Simultaneously
0 & 1

Entanglement

Simultaneously
00 & 01 & 10 & 11
Exponential factor

N qubits = 2^N classical bits

Number of states exponentially increase ➔ Astronomically large computing power

Quantum World: Key Concepts

Fragility

Observation or noise

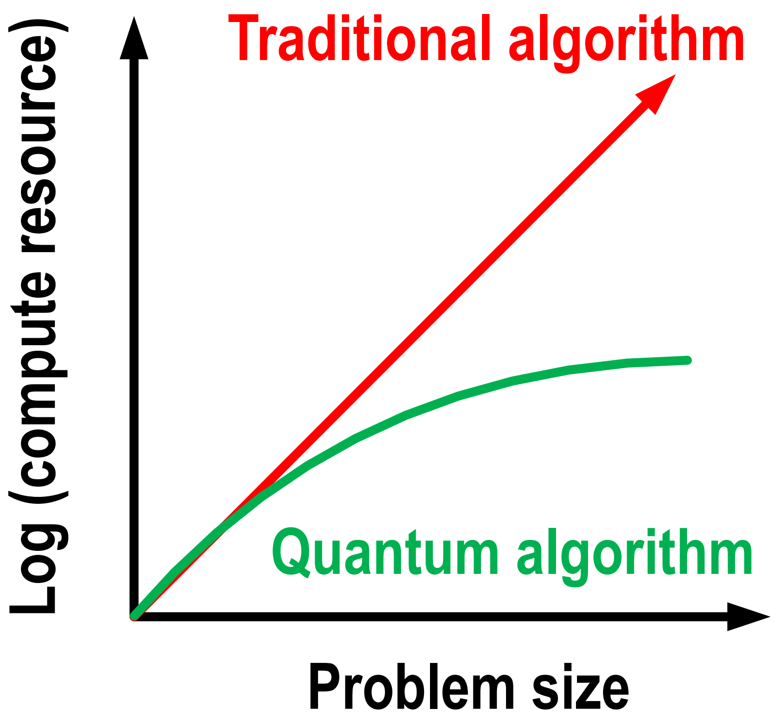
Quantum state collapse to classical state if observed or disturbed by noise

Decoherence time

Fragility → No cloning → Quantum Communication

Potential Applications vs Number of Qubits

- 50 entangled qubits
  - More states than any possible supercomputer (2^{50}) ➔ Quantum supremacy
- 300 entangled qubits
  - More states than atoms in this universe
- 1000 qubits with limited or no error correction
  - Quantum chemistry
  - Quantum neural networks
  - Optimization
- 1 million qubits **with full error correction**
  - Factoring/cryptography
  - Large linear systems
  - Unstructured search



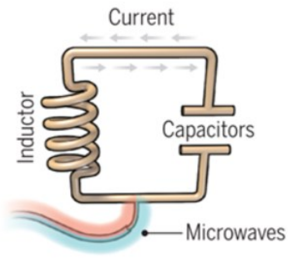
Exponential speed up compared to classical algorithms in some applications

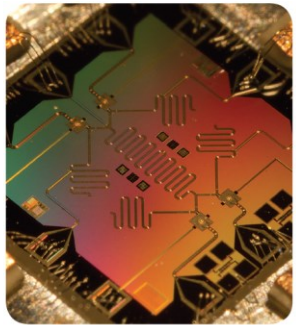
DiVincenzo Criteria for Building Quantum Computer

- Well defined and addressable quantum bits (qubits)
- Can be initialized reliably in a simple fiducial state (e.g. ground state)
- Universal set of gates
- Long decoherence time (>> gate-operation time)
- Reliable, qubit-specific measurement capability

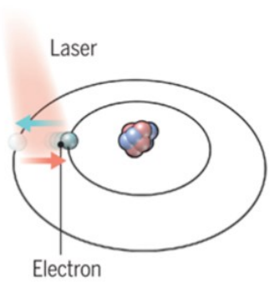
Quantum Technologies Compared

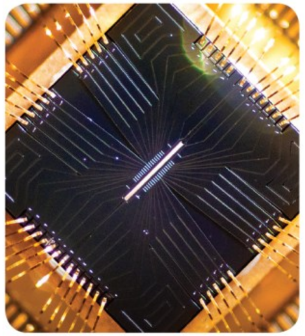
Superconducting qubits



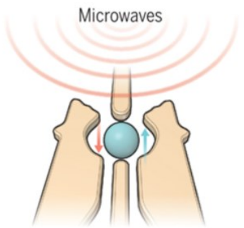


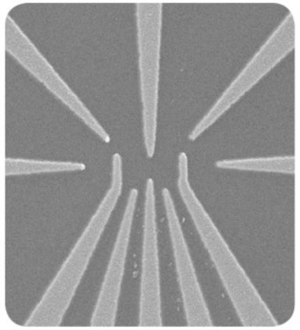
Trapped ions





Silicon quantum dots

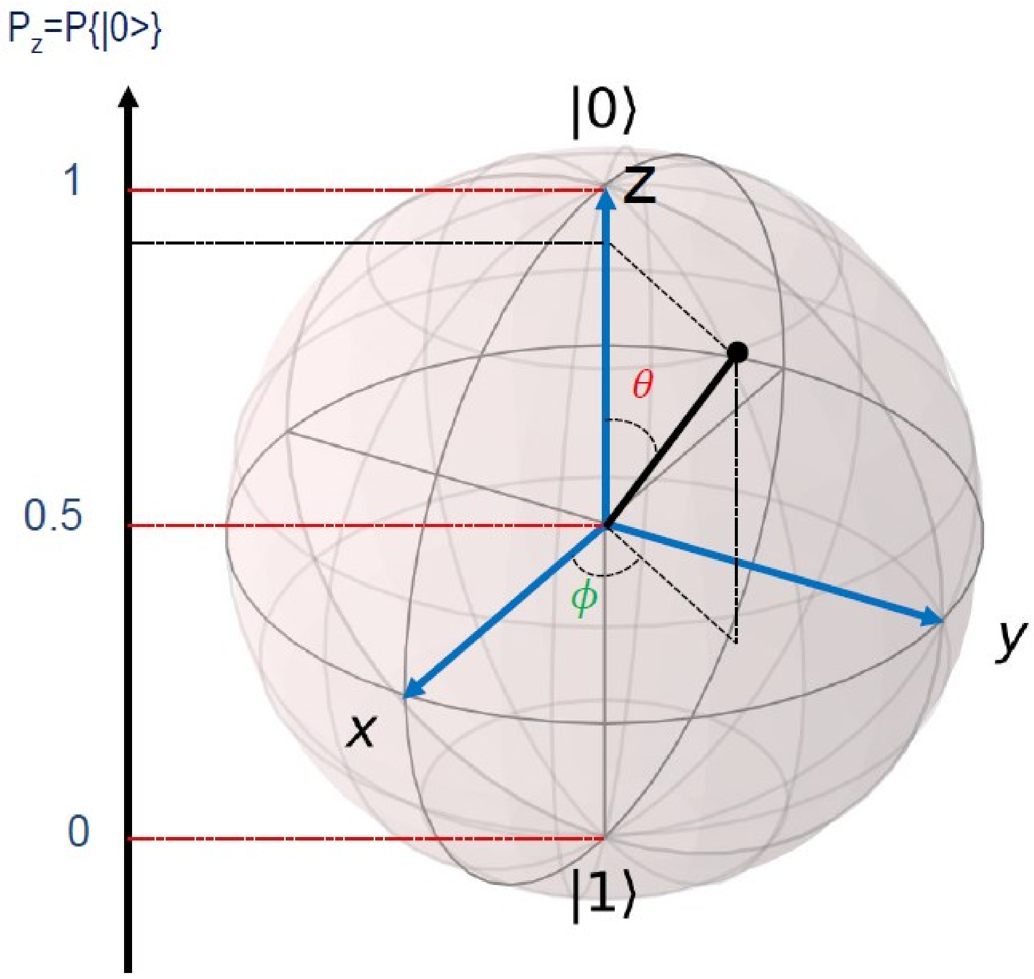




Size	100μm^2	1mm^2	100nm^2
Fidelity	99.3%	99.9%	98%
Speed	100ns	100μs	5μs
Variability	3%	0.0001%	0.1-0.5%
Temperature	50mK	300K	0.1-1K
Companies	**Google, IBM, Rigetti, DWave**	**Honeywell, IonQ**	**Intel Corporation, HRL**

Ref: Mathilde IMS 2021, Morton and Lo IEEE Spectrum

Qubit States & Control



- North pole
  - Ground state $|0\rangle$
- South pole
  - Excited state $|1\rangle$
- Any point on the sphere
  - Pure state

$$\psi = cos\left(\frac{\theta}{2}\right) + e^{i\phi} sin\left(\frac{\theta}{2}\right)|1\rangle$$

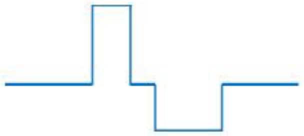
- Qubit state probability
  - Z-axis projection $P\{|0\rangle\} = cos^2\left(\frac{\theta}{2}\right)$
- Z axis rotation ϕ done in software
- XY axis rotation θ done in controller

A Fully-Integrated Cryo-CMOS SoC for Qubit Control in Quantum Computers Capable of State Manipulation, Readout and High-Speed Gate Pulsing of Spin Qubits in 22nm FinFET Technology", IEEE ISSCC 2021

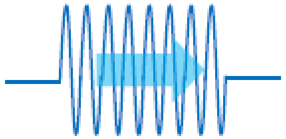
Control Electronics for Quantum Computing

- Mapping software instruction into electrical signals
  - Manipulate qubit states (drive/write)
    - RF pulses (shaped)

  - Control qubit-to-qubit interactions (entanglement)
    - Square pulses

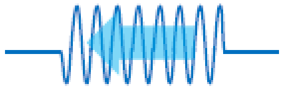


  - Read qubit state (readout)
    - Generate RF pulse



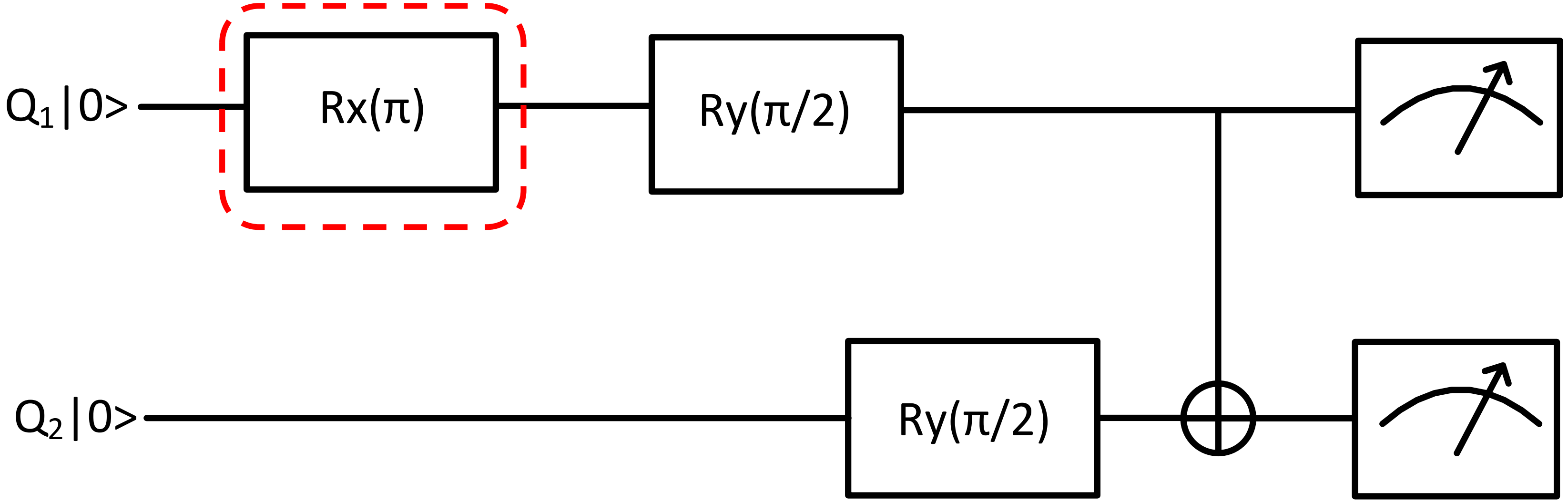
Stimulus

    - Detect amplitude and phase shift in reflected pulse

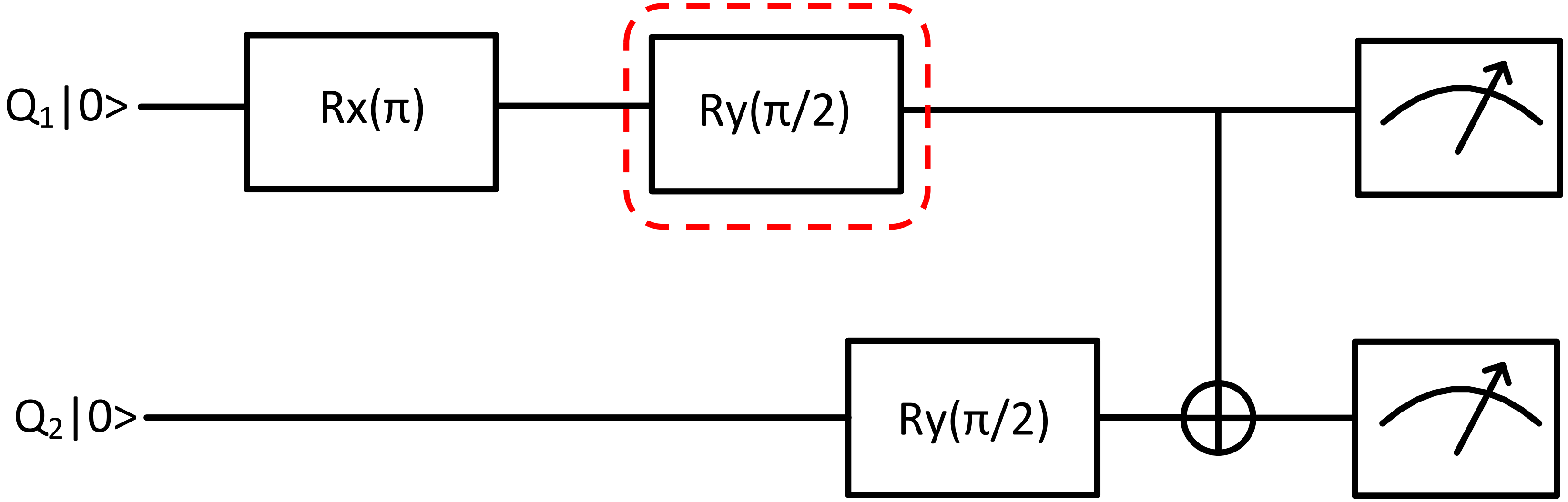


Reflected

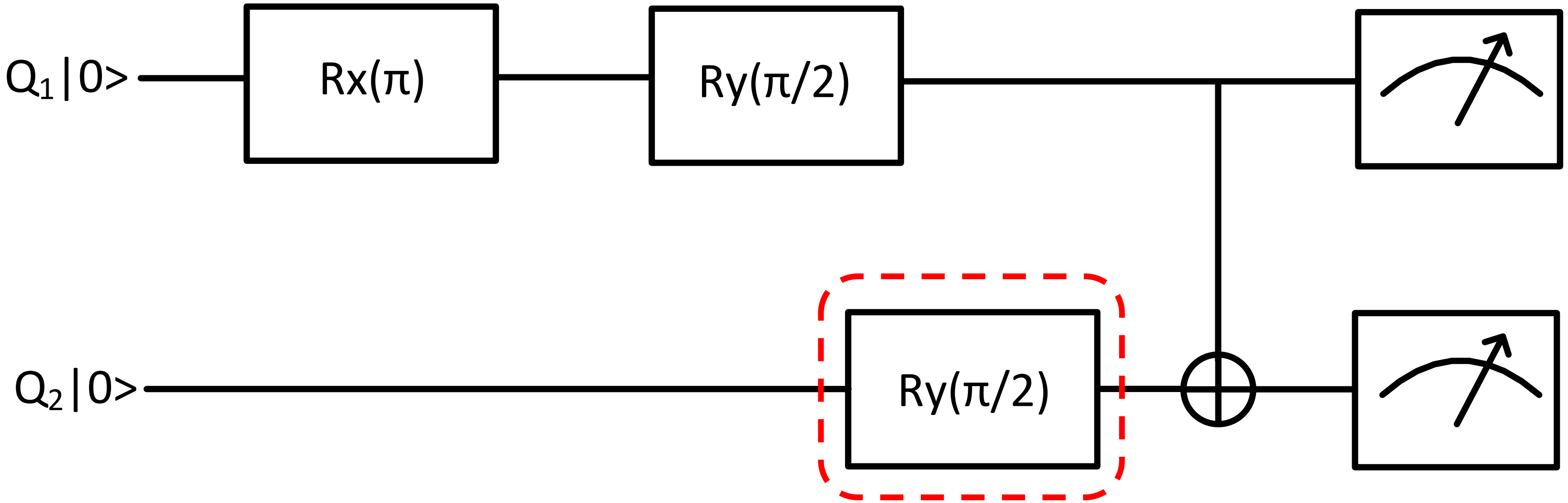
Single Qubit Operation (1/3)



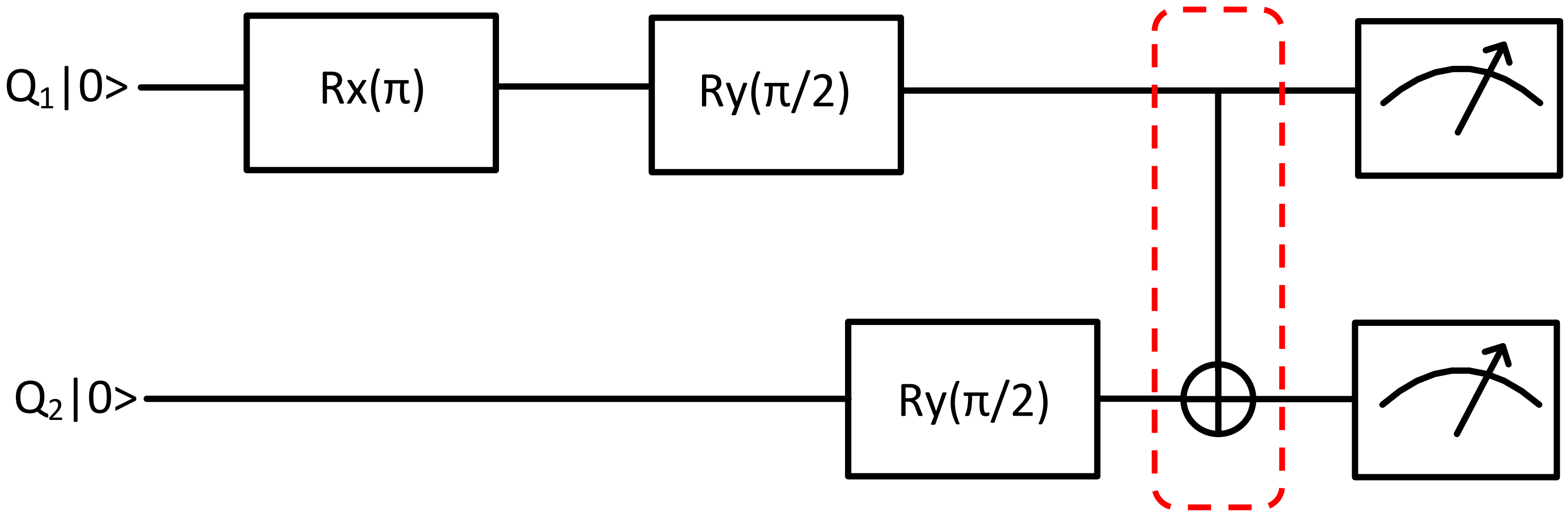
Single Qubit Operation (2/3)



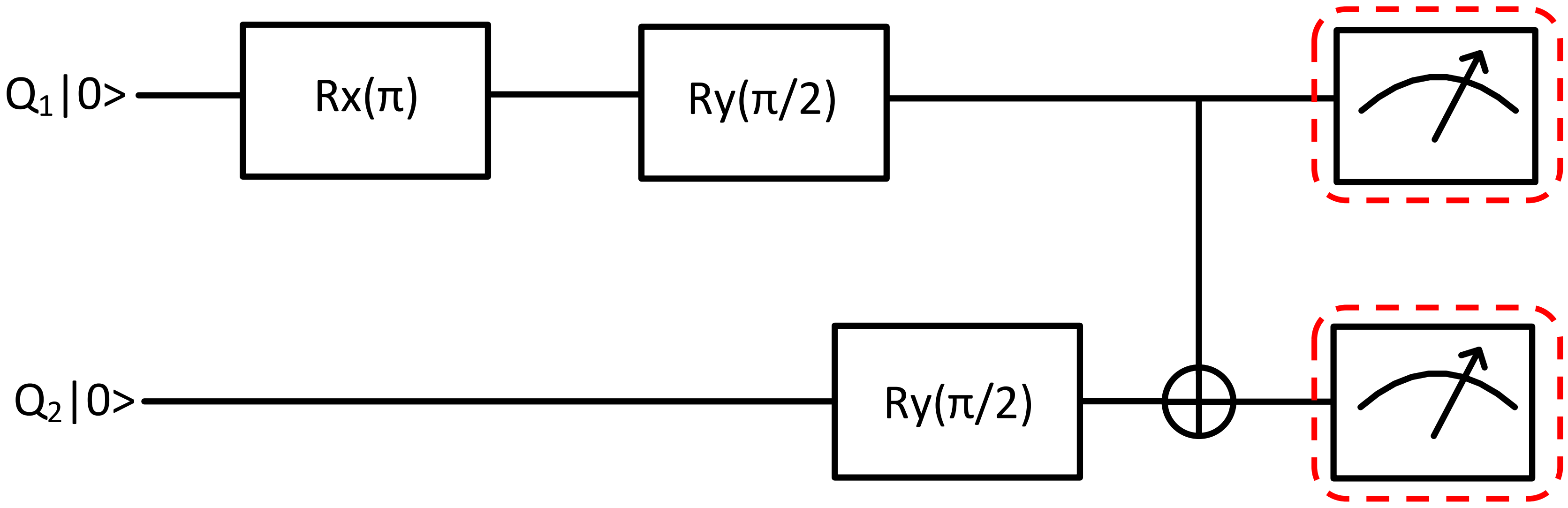
Single Qubit Operation (3/3)



Two Qubit Operation (1/2)

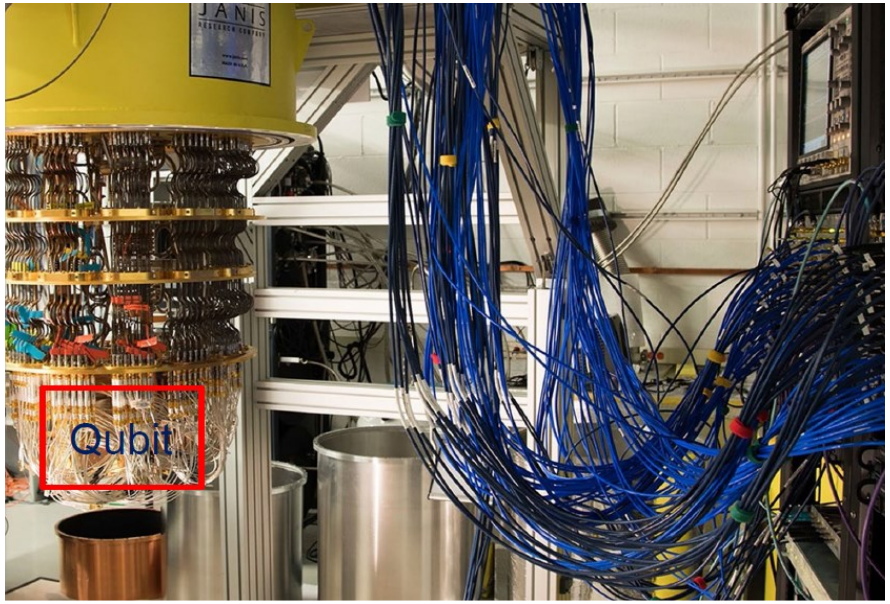


Two Qubit Operation (2/2)



Scaling to Many Qubits

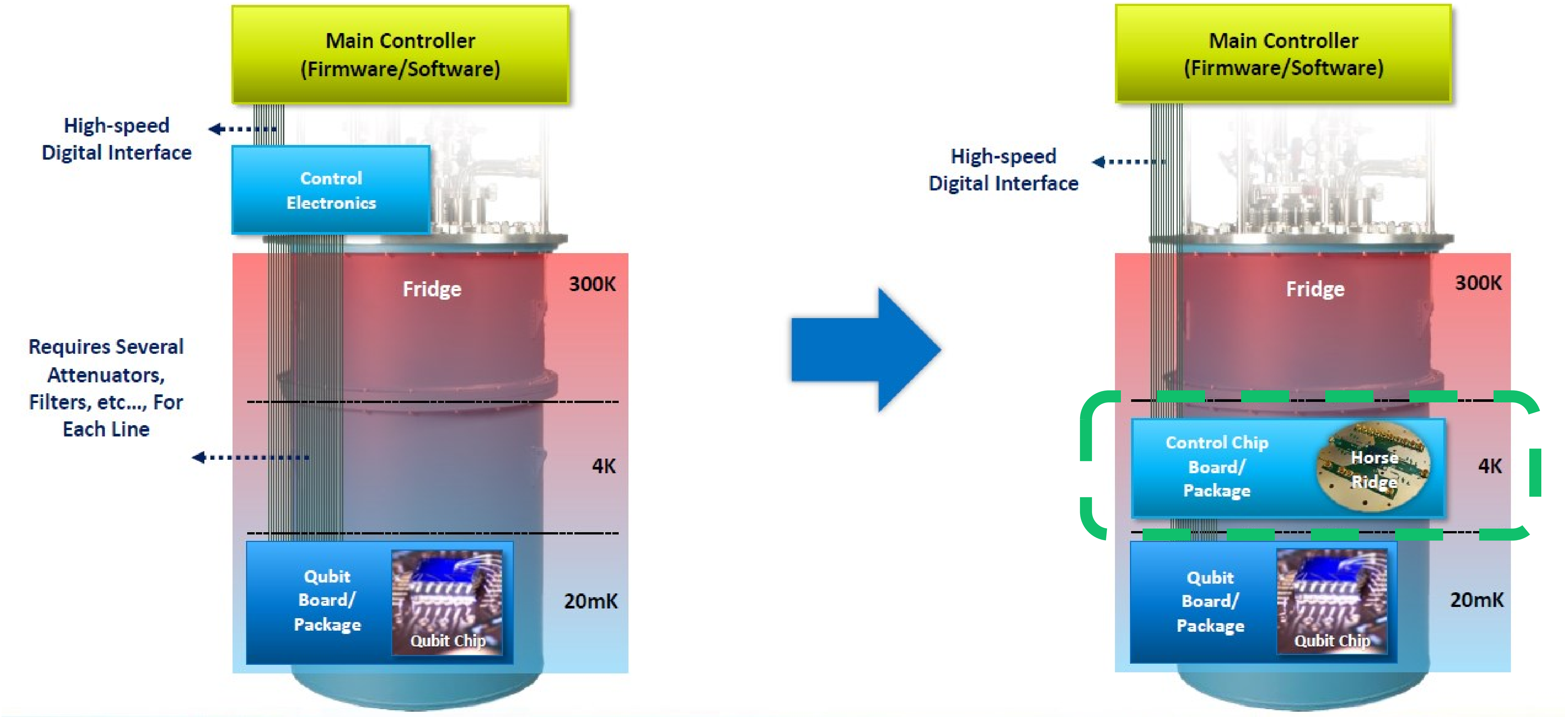
- Present quantum computer status
  - Qubits in dilution refrigerator controlled by room temperature test equipment using coaxial cables
  - Requires at-least 2 coaxial cables/ qubit➔ interconnect complexity, reliability issue
  - Huge form factor ➔ Bulky room temp. test equipments
  - Heavy thermal load on the fridge
  - Power consumption and cost



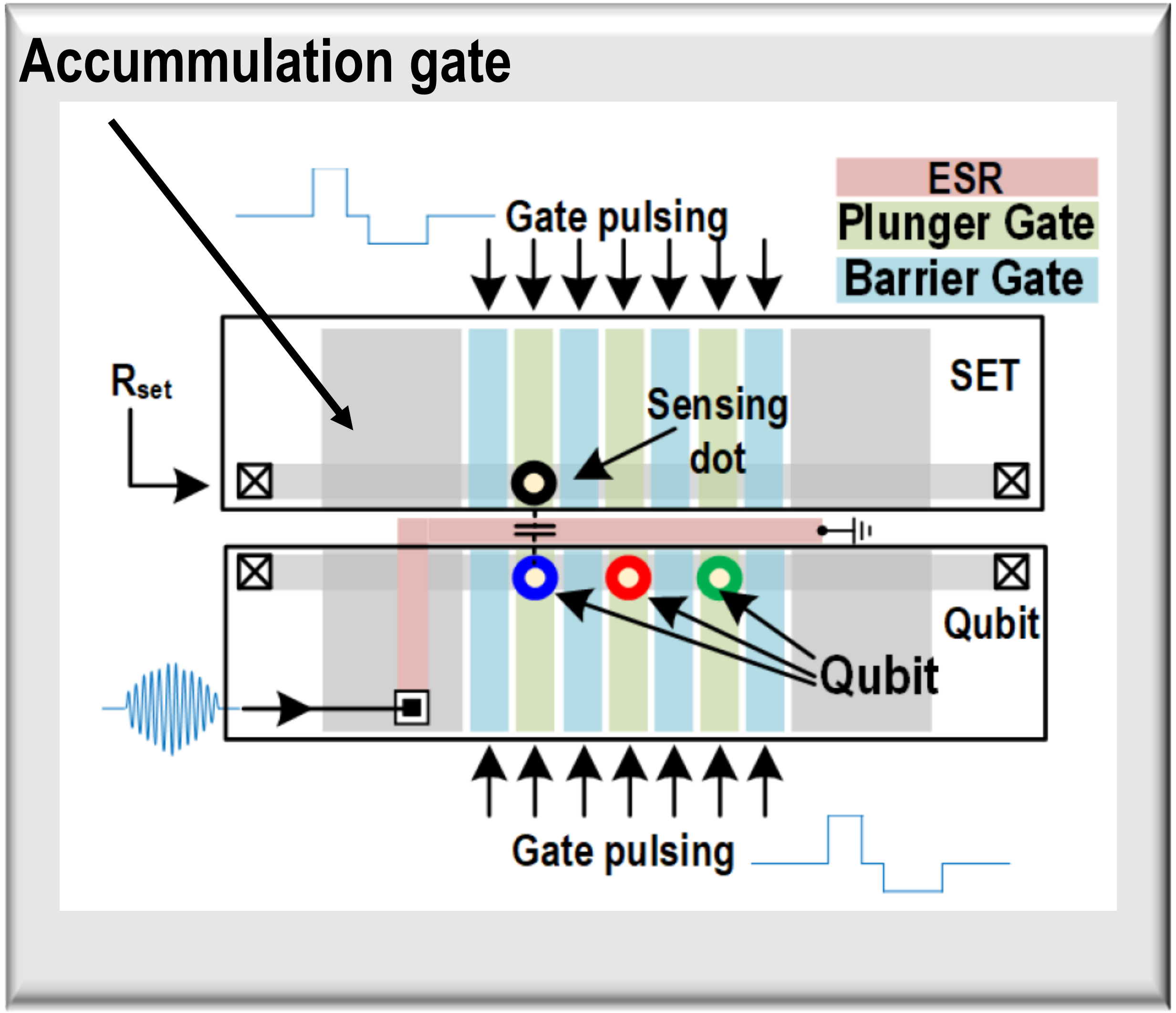
Bardin, ISSCC 2019: Present approach

- **Present approach with external control electronics does not scale with no. of qubits!!**
- **Proposal : Integrated CMOS controller IC placed at 4K to solve scalability problems**

Scaling to Many Qubits



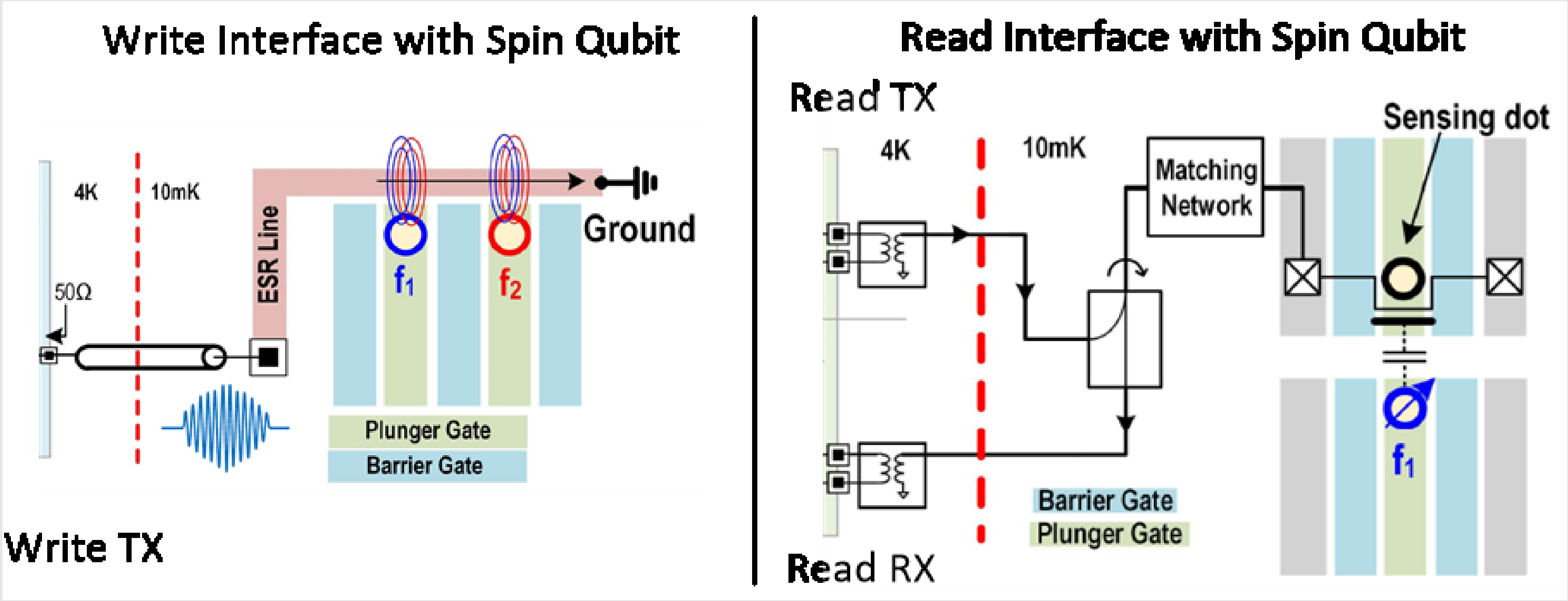
Spin Qubit Control Signals



- Biasing & entanglement
  - Plunger gate (qubits are formed)
  - Barrier gate (qubit coupling)
  - Square pulses
- Write/ Drive qubit state
  - ESR line (Electron spin resonance)
  - RF pulses
- Read qubit state [spin up (R1) & down (R0)]
  - Accumulation gate
  - Generate stimulus pulse
  - Detect amplitude & phase of reflected pulse

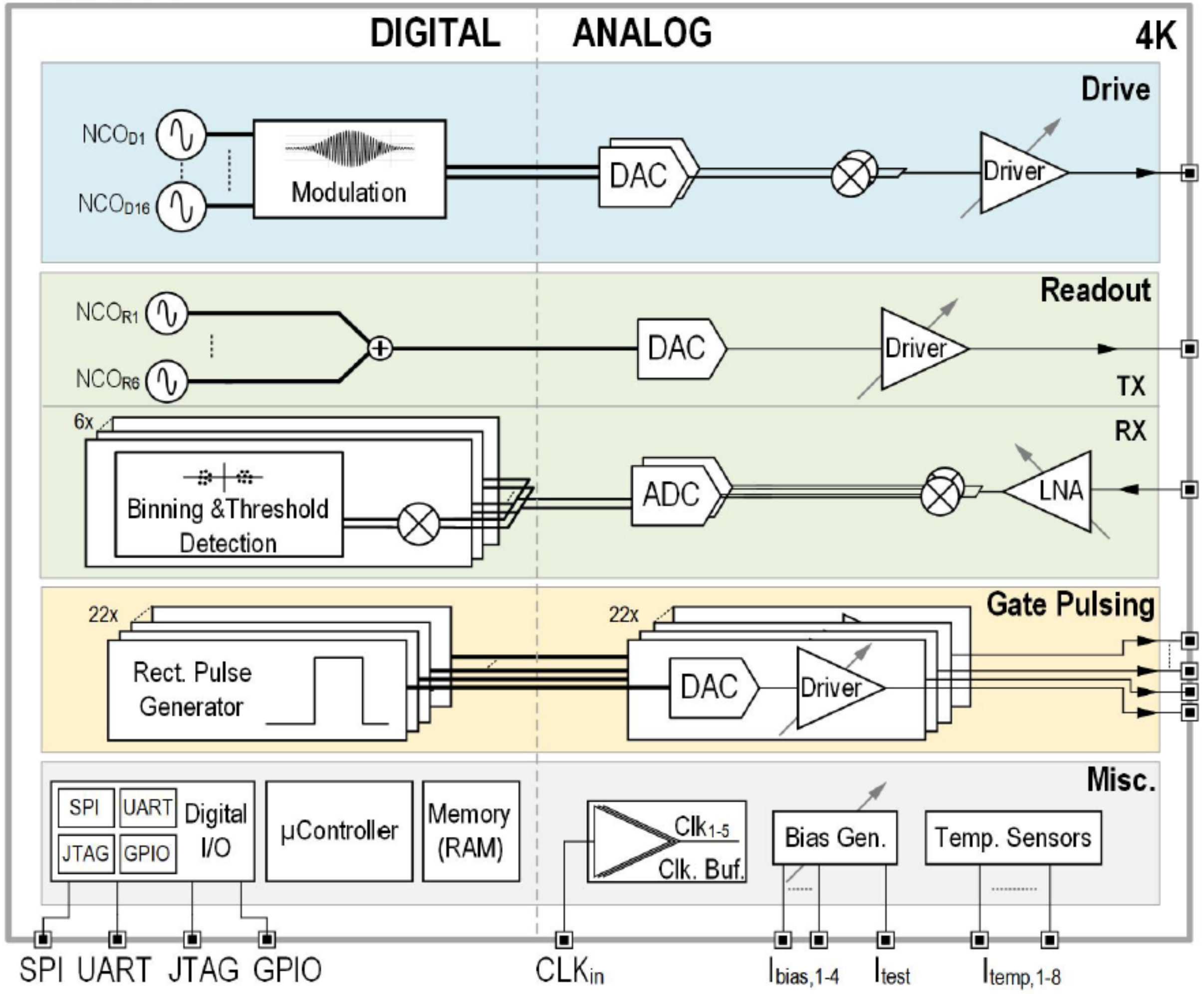
A Fully-Integrated Cryo-CMOS SoC for Qubit Control in Quantum Computers Capable of State Manipulation, Readout and High-Speed Gate Pulsing of Spin Qubits in 22nm FinFET Technology", IEEE ISSCC 2021

Read/Write Interface with Spin Qubits



[1] A Fully-Integrated Cryo-CMOS SoC for Qubit Control in Quantum Computers Capable of State Manipulation, Readout and High-Speed Gate Pulsing of Spin Qubits in 22nm FinFET Technology", IEEE ISSCC 2021
[2] J. Park et al., "A Fully Integrated Cryo-CMOS SoC for State Manipulation, Readout, and High-Speed Gate Pulsing of Spin Qubits," IEEE Journal of Solid-State Circuits, Nov, 2021 (invited)

System Level Block Diagram: Superconducting & Spin Qubits



- Drive: Microwave pulse generation
- RF reflectometry readout: Multitone signal generation and detection of reflected signal
- Gate pulsing: Square pulse generation
- Integrated microcontroller
- Integrated temperature sensing
- 16 write/ 6 read (FDMA)

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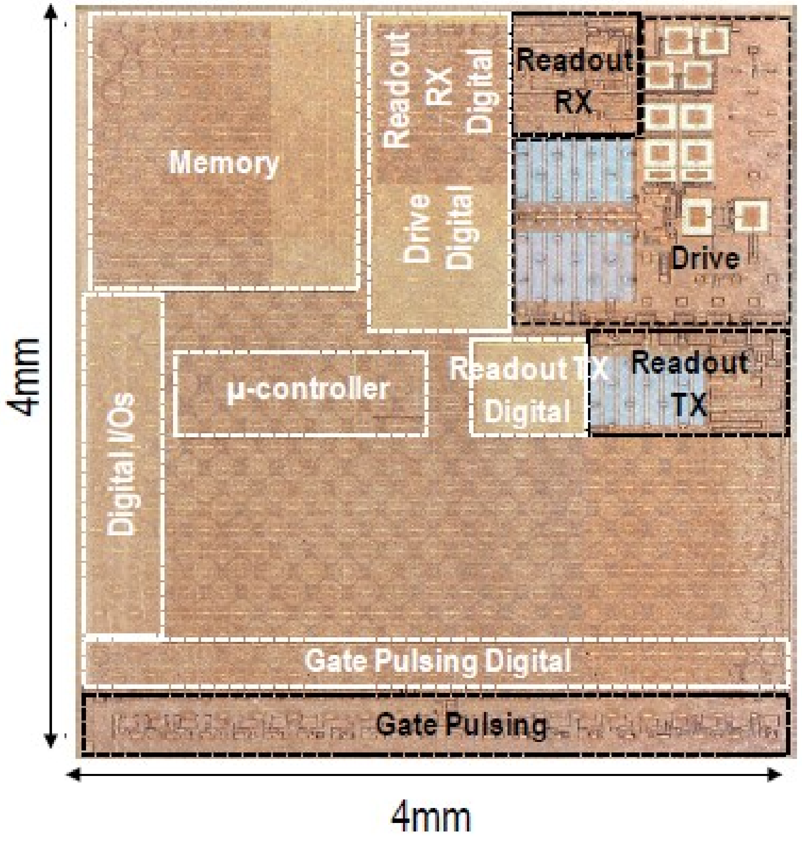
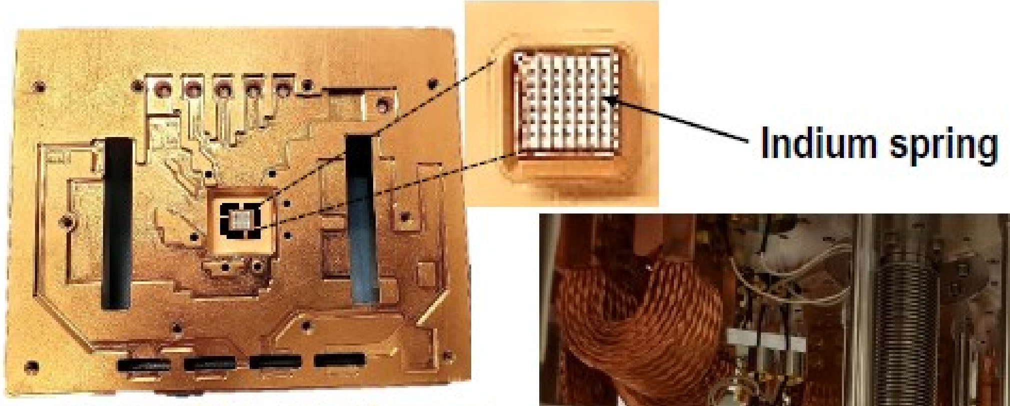
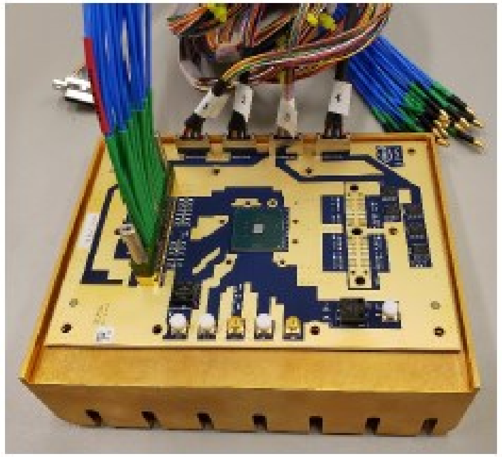
Challenges in Cryogenic Controller IC Design

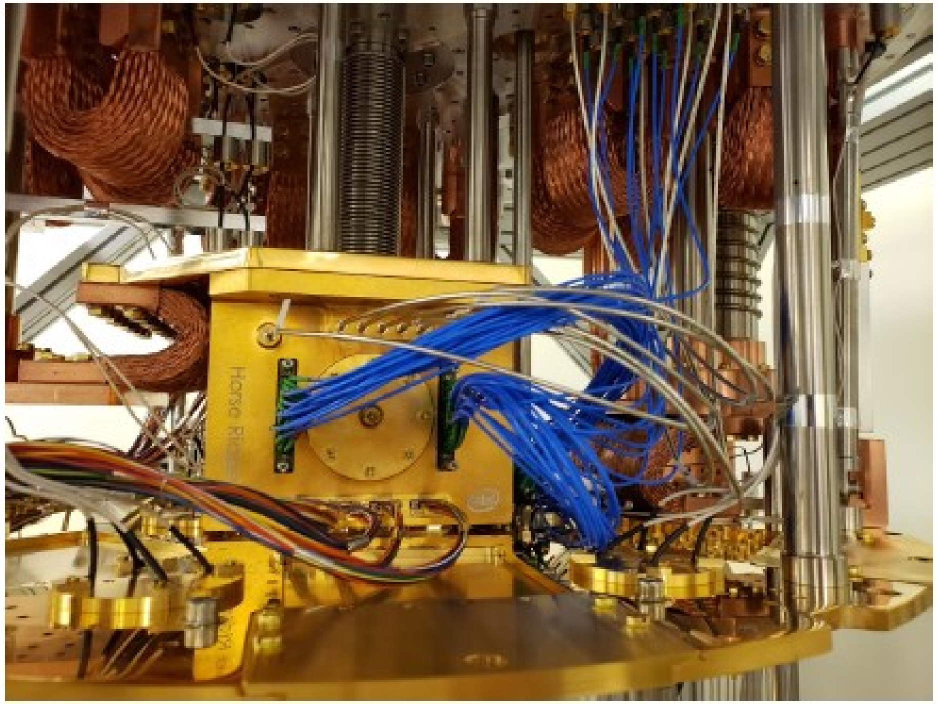
- Enable System-on-Chip (SoC) Design at Cryogenic Temperature
  - Low power
  - Achieve high fidelity
  - Number of controllable qubits
- Identify Signal Specifications
- Fully-Scalable Architecture
- Cryogenic Packaging
- Mechanical and Thermal Integration

SoC Controller & Measurement Setup









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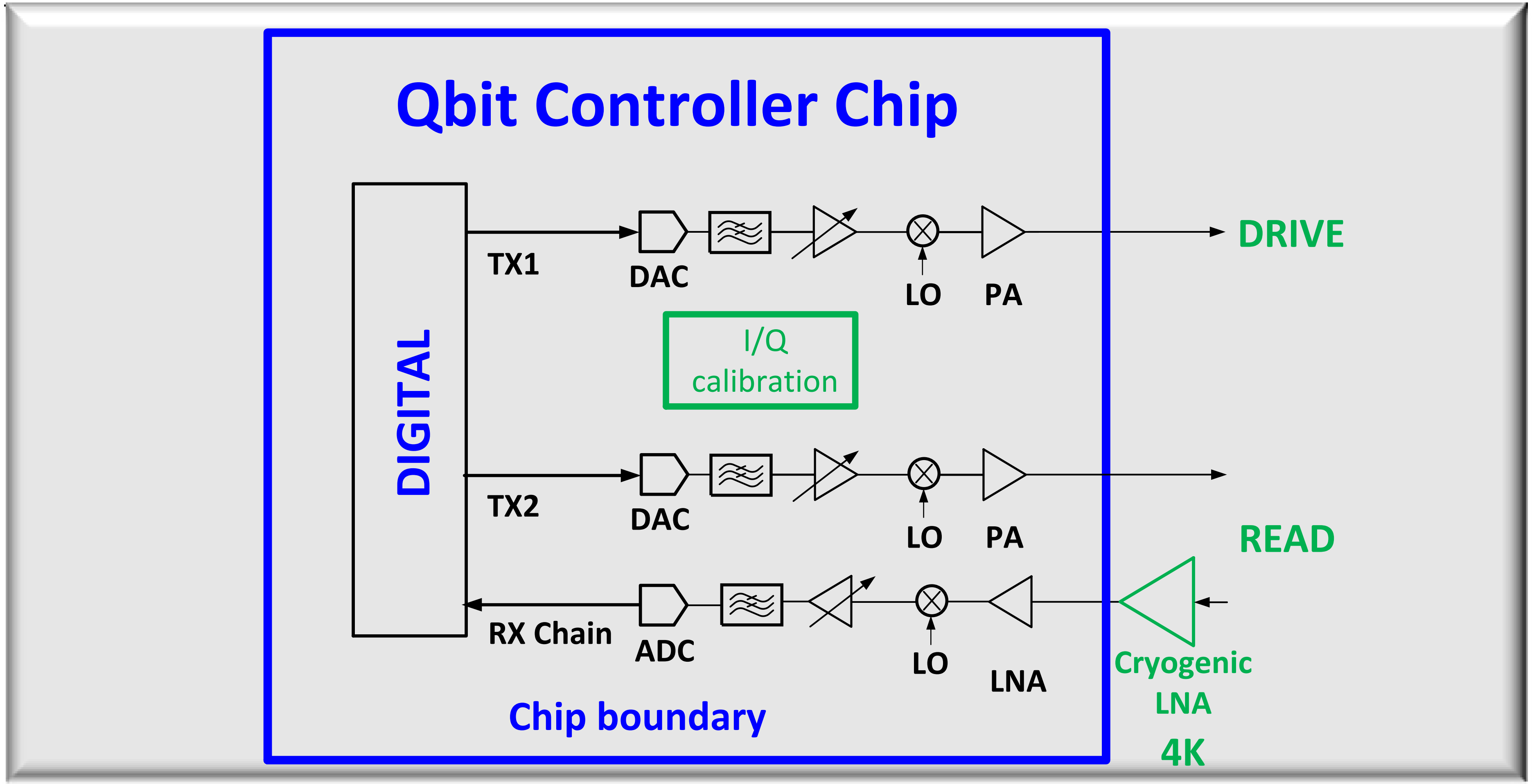
IIT Delhi ARIL Hardware

- CMOS cryogenic controller chip in TSMC 28nm for ***both superconducting & spin qubits***
- State-of-the-Art power and number of controllable qubits



Conclusion

- Controlling qubits ➔ High precision RF/analog signals
- Large number of coax cables into the fridge ➔ current approach does not scale
- Scaling of QCs supported by cryogenic controller IC
- Cryogenic ICs promising to replace room temperature control approach
- Cryogenic controller IC is key to realizing Quantum Computer
- IIT Delhi ARIL is developing controller chip for both superconducting & spin qubits

THANK YOU!