Centre for Programmable Photonic Integrated Circuits and Systems

(CoE-CPPICS, Funded by MeitY, Govt. of India)

Quantum Efforts

Bijoy Krishna Das

Chief Investigator, CoE-CPPICS

&

Professor in Department of Electrical Engineering, IIT Madras

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- **Background, Scopes and Objectives**
- **Team, Infrastructure and Facility**
- **Silicon Photonics: Quantum Technology**

CPPICS : Background, Scopes and Objectives

15 Years of Silicon Photonics Research @ IIT Madras

2007 → 2022

2006 — Establishment of Integrated Optoelectronics Lab (IIT Madras Seed Funding Rs. 5L)

2008 — First funded projects on Silicon Photonics (DRDO, DST, DIT)

2009 — Demonstration of 5 µm SOI optical waveguide

2010 — First MS thesis on Silicon Photonics

2011 — Demonstration of packaged Silicon Photonics devices (5 µm SOI)

2012 — Funding for Silicon Photonics Nanotechnology (CNNP/MeitY, DRDO)

2013 — Demonstration of Silicon Photonics active devices (PIN waveguide, 5 µm SOI)

2014 — Demonstration of spot size converter (Microns to sub-micron waveguides)

2015 — Demonstration of surface trimming of devices using controlled RIE

2016 — First international patent filed, first PhD graduation

2017 — First publication on CMOS compatible Silicon Photonics devices (220 nm SOI)

2018 — Demonstration of CMOS compatible reconfigurable Silicon Photonics devices

2019 — Demonstration of FWM in Silicon photonic wire waveguide devices

2020 — Demonstration of high extinction on-chip pump rejection filters

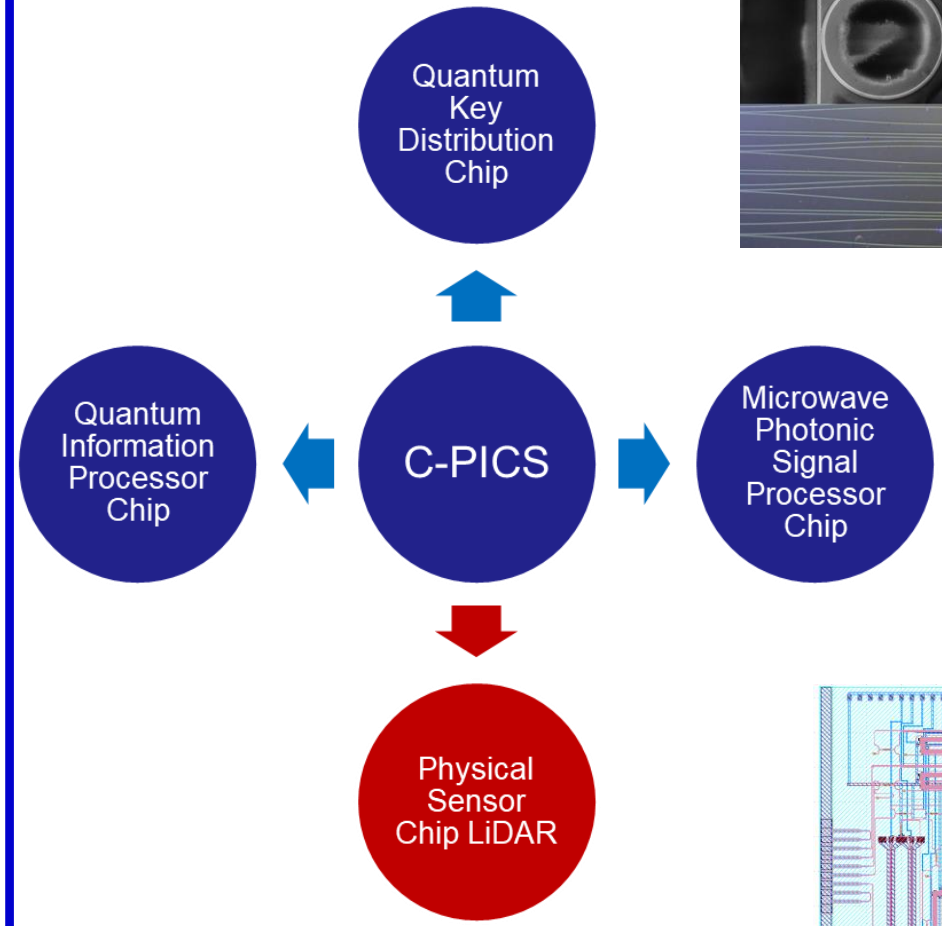
2021 — **6 PhD and 15 MS Graduated**

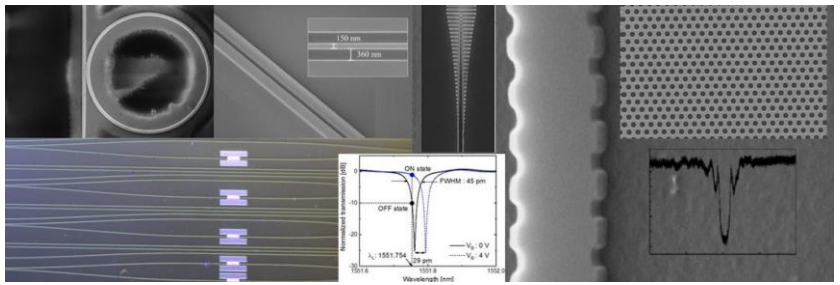
IoE-pCoE
MeitY CoE-CPPICS

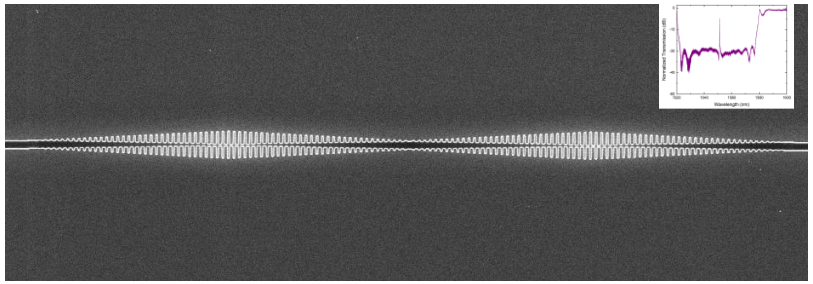
Status in 2022: 4 Research Associates, 12 PhD and 3 MS Research Scholars and 7 Project Staff

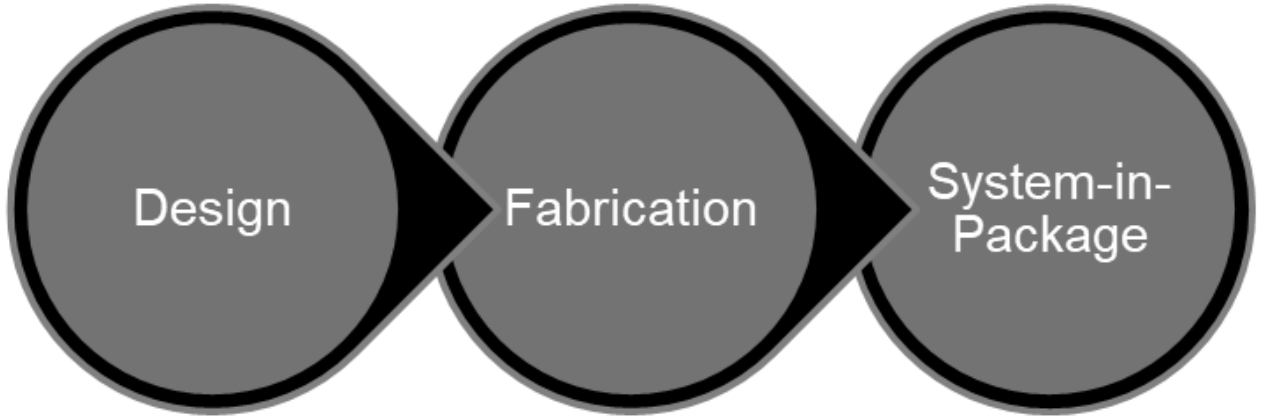
CPPICS : Background, Scopes and Objectives

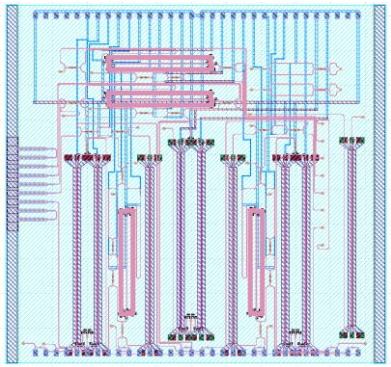
Pushing Silicon Photonics Technology: PICS Product Research Development and Manufacturing Model

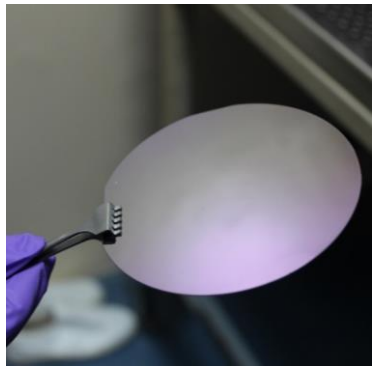


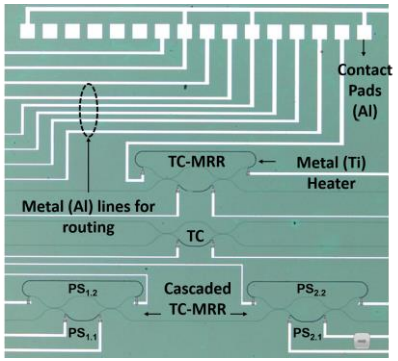


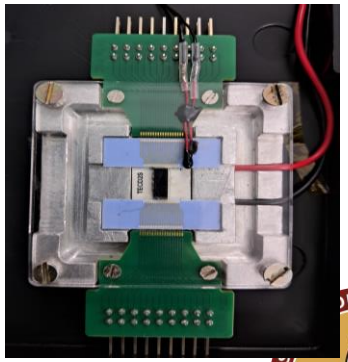












CPPICS : Team, Infrastructure and Facility

Scopes: PICS Design, Fabrication, Testing & Packaging

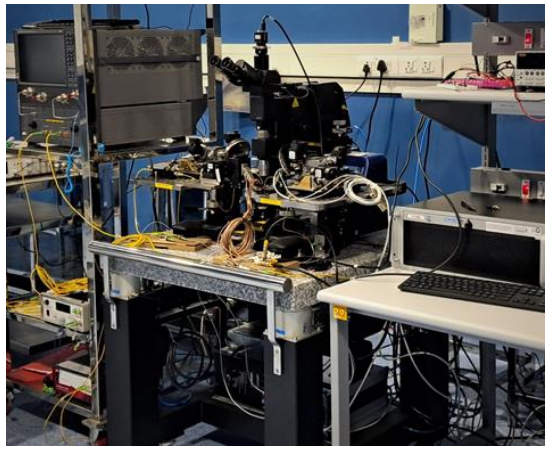
Cleanroom facilities spreading over 5000 Sq.ft.

Design & Simulation Tools:

- ❑ Ansys Lumerical
- ❑ Cadence Photonics
- ❑ COMSOL Multiphysics
- ❑ Synopsys Sentaurus

Major Process Tools for Silicon Photonics:

- ❑ Upgraded E-Beam Lithography
- ❑ DUV Lithography Mask Aligner
- ❑ ICP RIE Systems
- ❑ E-beam Deposition Systems
- ❑ LPCVD and PECVD Systems
- ❑ Oxidation and Diffusion Furnaces
- ❑ Chemical Mechanical Polishing



2500 sq. ft. of Design and Characterization Labs

Major Characterization Tools:

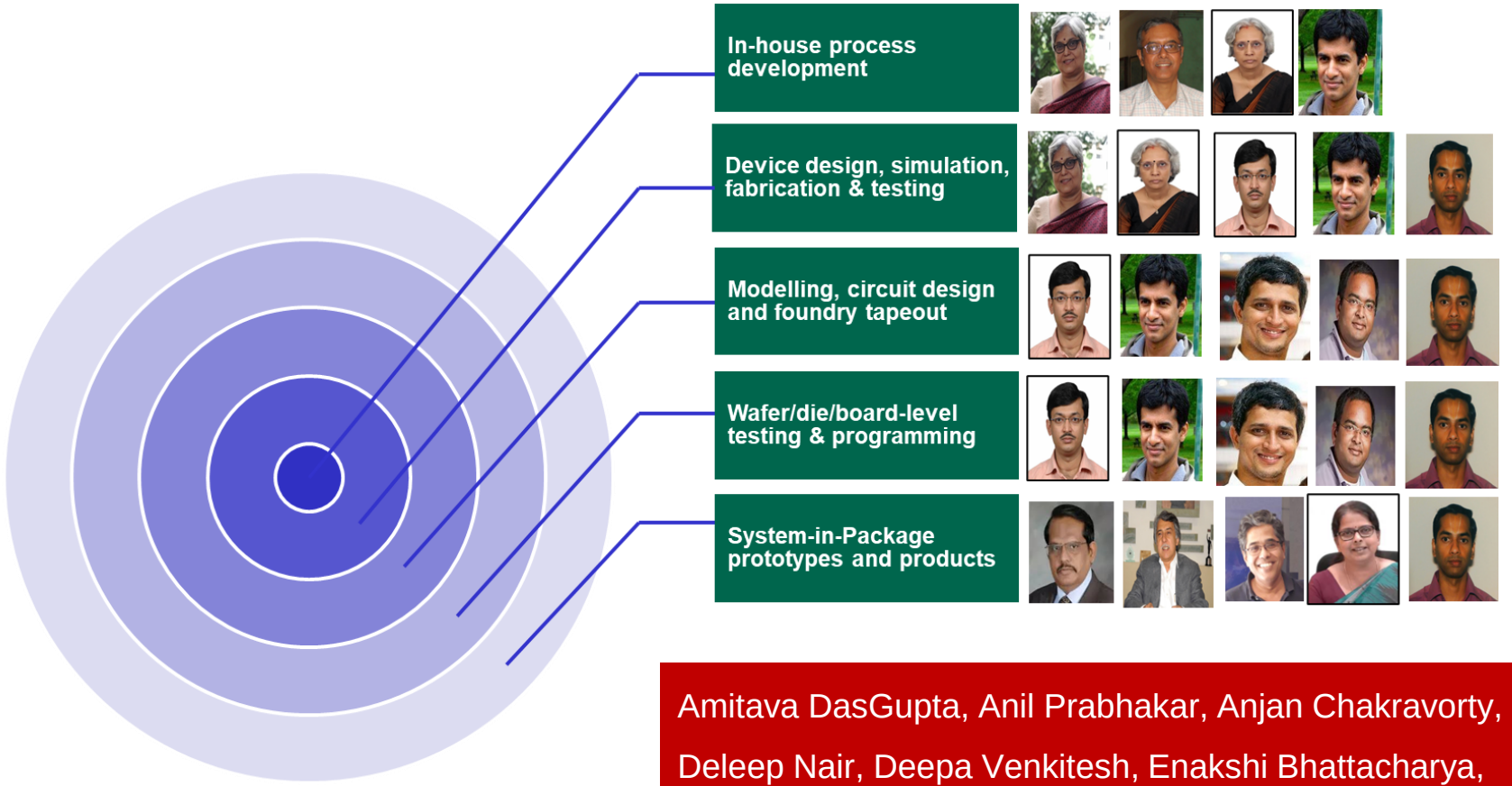
- ❑ Indigenous chip-scale silicon photonics probe station
- ❑ Silicon photonics probe station for die-level testing
- ❑ RF Phase Noise Analyzer
- ❑ Fully automated wafer-scale silicon photonics probe station
- ❑ 8 Channel SNSPD for testing Quantum Photonics Chips
- ❑ Light Component Analyzer for e/o and o/e device characterization
- ❑ High Resolution Source Optical Spectrum Analyzer
- ❑ Fiber Pigtailing and Packaging Setup

CPPICS : Team, Infrastructure and Facility

Chief Investigator

Chief Technology Officer

Team CoE-CPPICS: Collaborating Faculty Members



Amitava DasGupta, Anil Prabhakar, Anjan Chakravorty, Deleep Nair, Deepa Venkitesh, Enakshi Bhattacharya, Janakiraman Viraraghavan, Nandita DasGupta, Saurabh Saxena, Sudharsanan Srinivasan

CPPICS : Team, Infrastructure and Facility

Industry Advisory Board for Guidance and Supports

CHAIRMAN

Dr. Mallik Tatipamula

CTO at Ericsson, San Jose, California, USA

Message from the Chairman-

I am delighted that the Centre of Programmable Photonic Integrated Circuit & Systems (CPPICS) has been engaged with cutting edge technology R & D activities under the leadership of Prof. Bijoy Krishna Das. The progress of CoE-CPPICS has been commendable during the last couple of years and its future R&D roadmap has been well planned complying with the immediate needs of silicon photonics/electronics industries. As the chairman of CPPICS Industry Advisory Board, I am committed to coordinate with other board members to provide guidance to the team CoE-CPPICS to continue its activities following the Product Research Development and Manufacturing Model.

Dr. Vivek Raghunathan

Founder & CTO
Xscape Photonics Inc., USA

Mr. Arjun Kumar Kantimahanti

Senior Vice President
SilTerra, Malaysia

Dr. Prith Banerjee

CTO, Ansys Inc.
Palo Alto, California, USA

Dr. Steve Johnston

Vice President
Merck KGaA Darmstadt, Germany

Dr. Ravi M. Bhatkal

Managing Director
India Element Solutions Inc, India

Mr. Dinanath Soni

Executive Director,
Si2 Micro System, India

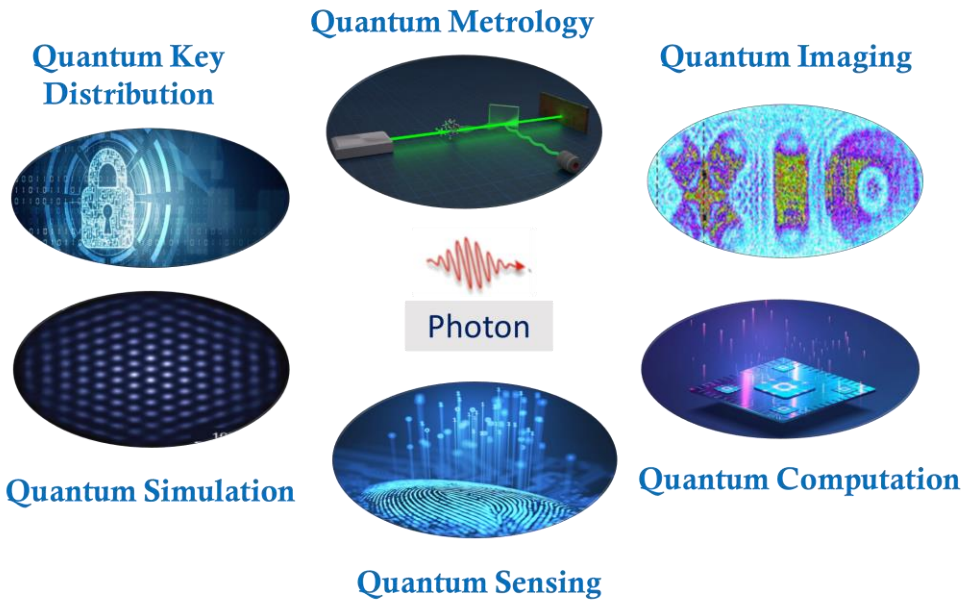
Mr. Kailash Narayanan
Vice President & General Manager
Keysight Technologies, USA

Mr. Vijay Janapaty
Vice President & General Manager
Broadcom Inc., USA

Mr. Vikas Gupta
Senior Director
Global Foundries, USA

CPPICS : Quantum Efforts

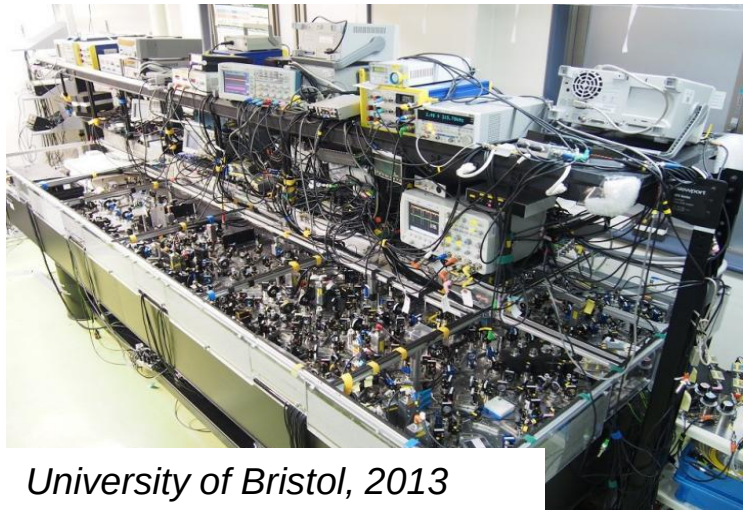
Quantum Photonics: Applications



Basic Optical Components

- Photon Sources
- Beam Splitter/Combiner
- Polarization Splitter/Combiner
- Interferometers
- Delay Lines
- Modulator/Switches
- Photon Detectors
- Control Electronics

Experimental Demonstration with Bulk Optics



University of Bristol, 2013

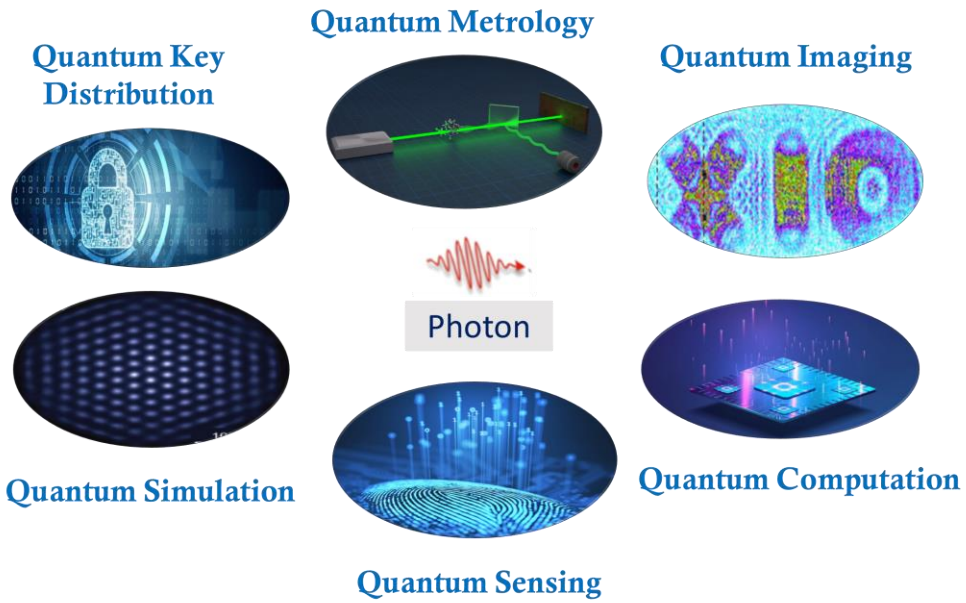
- Room Size Expt Setup
- Laborious & Time Consuming
- Stability Issue
- Not Scalable

Fundamental requirements

- Single Photon States
- Photon Superposition States
- Photon Entanglement States

CPPICS : Quantum Efforts

Quantum Photonics: Applications



Basic Optical Components

- Photon Sources
- Beam Splitter/Combiner
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- Control Electronics

Quantum Photonic Integrated Circuit

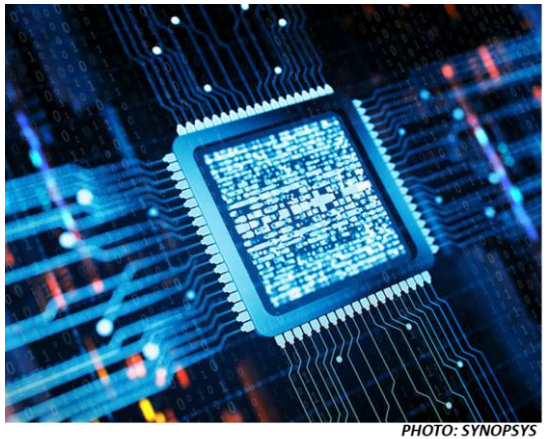


PHOTO: SYNOPSYS

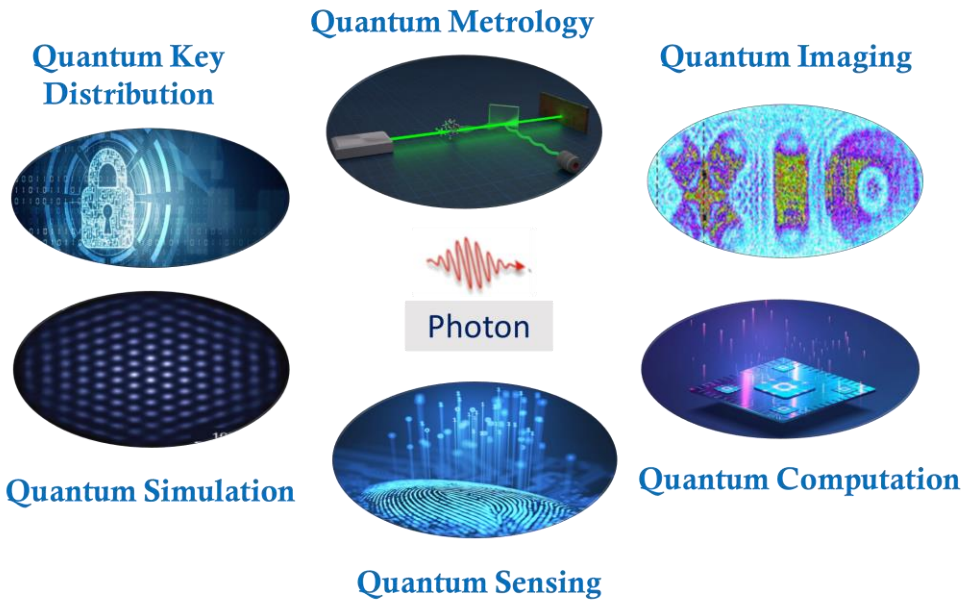
- Size/Compactness
- Stability
- Flexible functionalities
- Scalable & Cost Effective
- Programmable

Fundamental requirements

- Single Photon States
- Photon Superposition States
- Photon Entanglement States

CPPICS : Quantum Efforts

Quantum Photonics: Applications



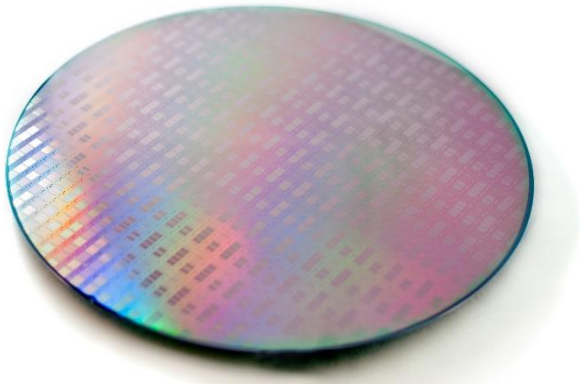
Basic Optical Components

- Photon Sources
- Beam Splitter/Combiner
- Polarization Splitter/Combiner
- Interferometers
- Delay Lines
- Modulator/Switches
- Photon Detectors
- Control Electronics

Fundamental requirements

- Single Photon States
- Photon Superposition States
- Photon Entanglement States

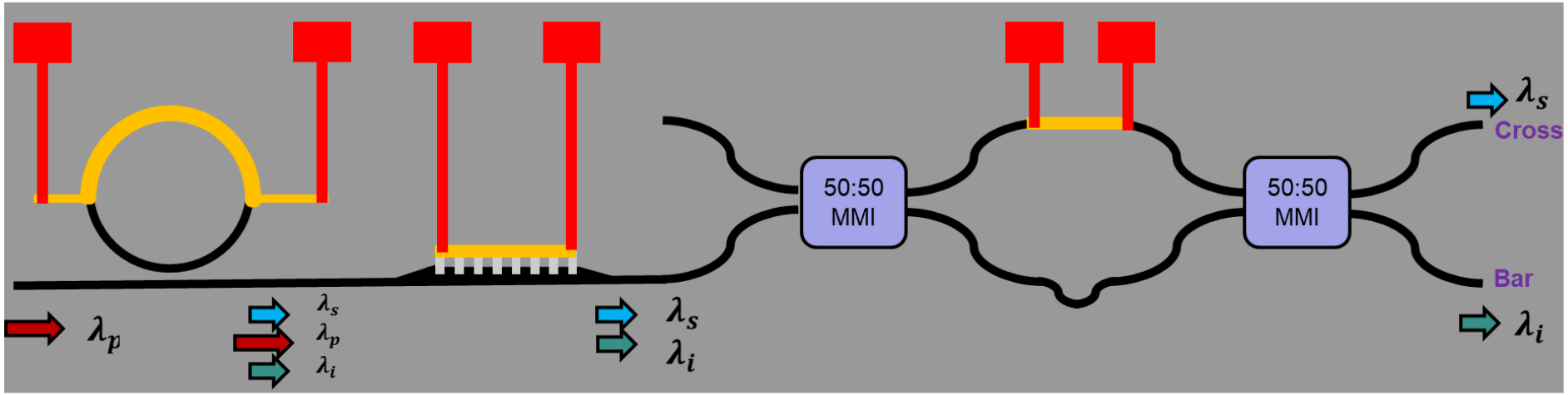
Silicon Photonics Platform



- CMOS Fabrication Process Compatible
- Integration of Electronics and Photonics
- High Confinement and Sharp Bends
- Photon Pair Generation through $\chi^{(3)}$

Top View

Photon Source Integrated with Pump Rejection Filter – Our Approach



Pump Rejection Filter

Photon Pair Separation

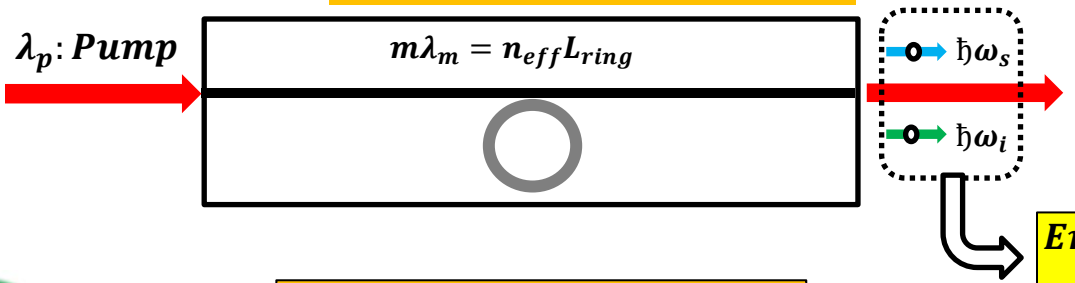
Si

SiO_2

TiN

METAL 2

Spontaneous Four Wave Mixing



λ_p: Pump to be attenuated ($> 100\ dB$)

Entangled or Correlated Photon Pairs

$\lambda_p \rightarrow \lambda_m; \lambda_s \rightarrow \lambda_{m-p}; \lambda_i \rightarrow \lambda_{m+p}$

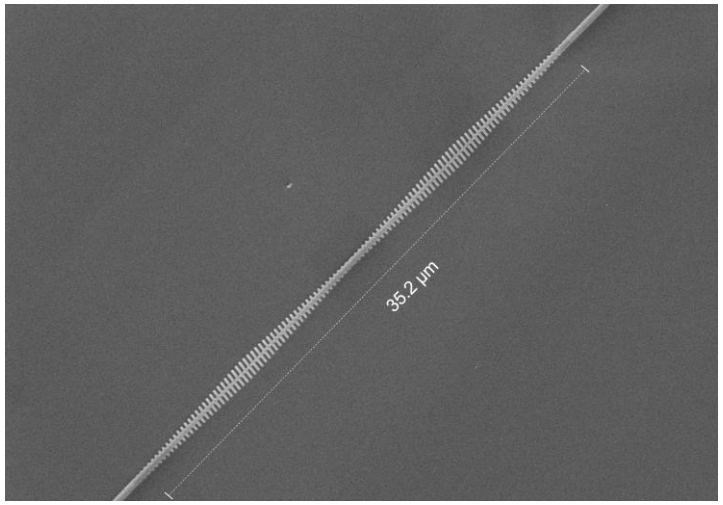
Generation Rate

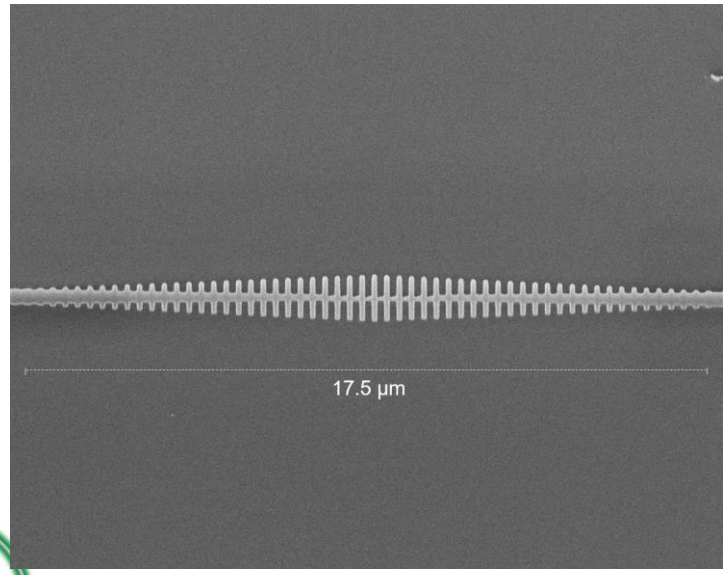
$$N_c = \frac{8v_g^4\gamma^2P_p^2Q^7}{\omega_r^3\pi^2R^2Q_e^4}$$

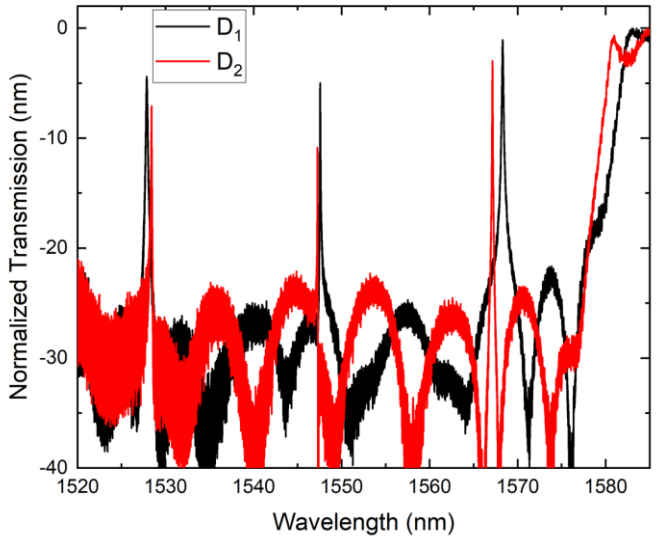
Brightness

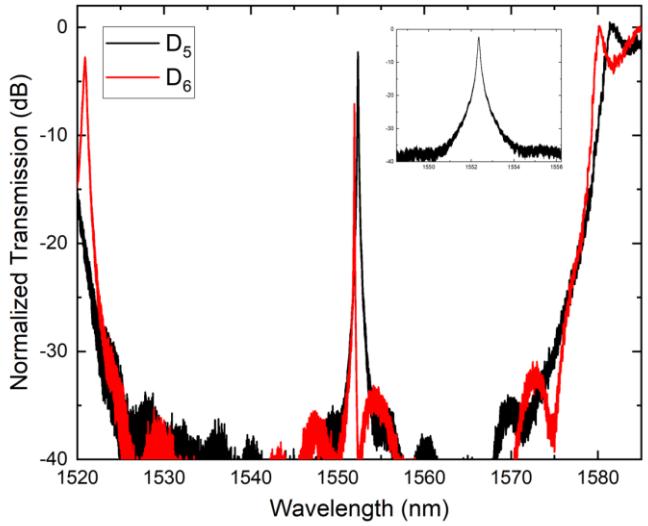
$$B = \frac{N_c}{P_P\Delta\lambda} = \frac{4v_g^4\gamma^2P_pQ^8}{\omega_r^2\pi^2R^2cQ_e^4}$$

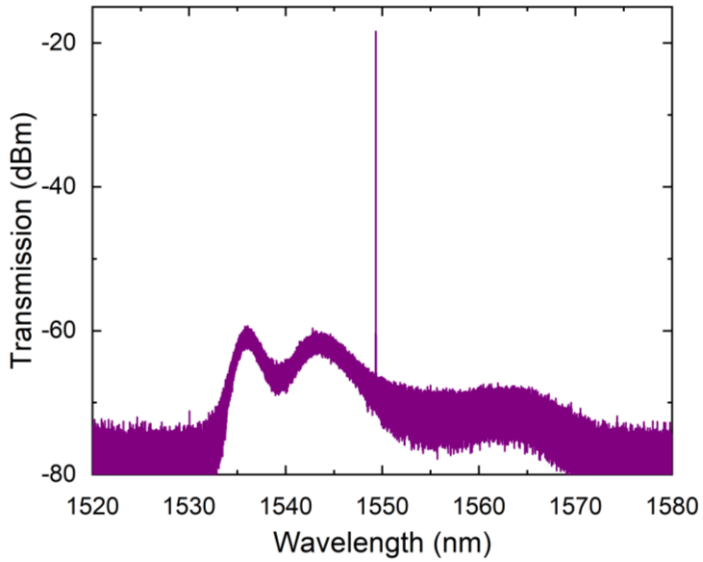
Photon Source Integrated with Pump Rejection Filter – Our Approach

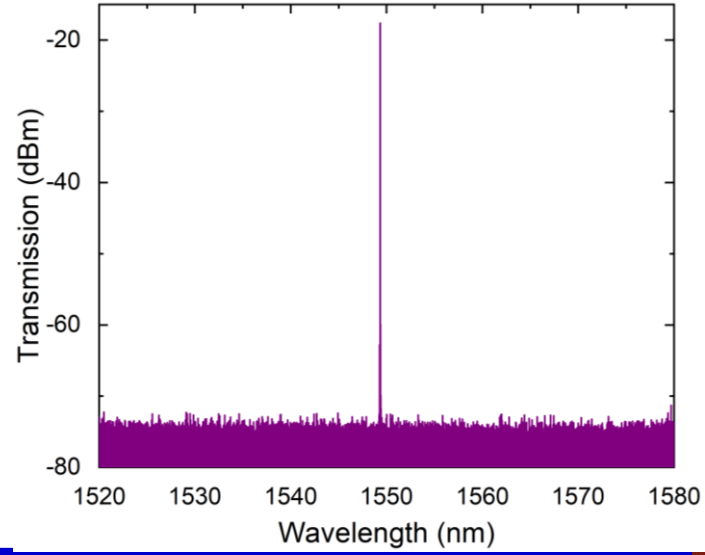










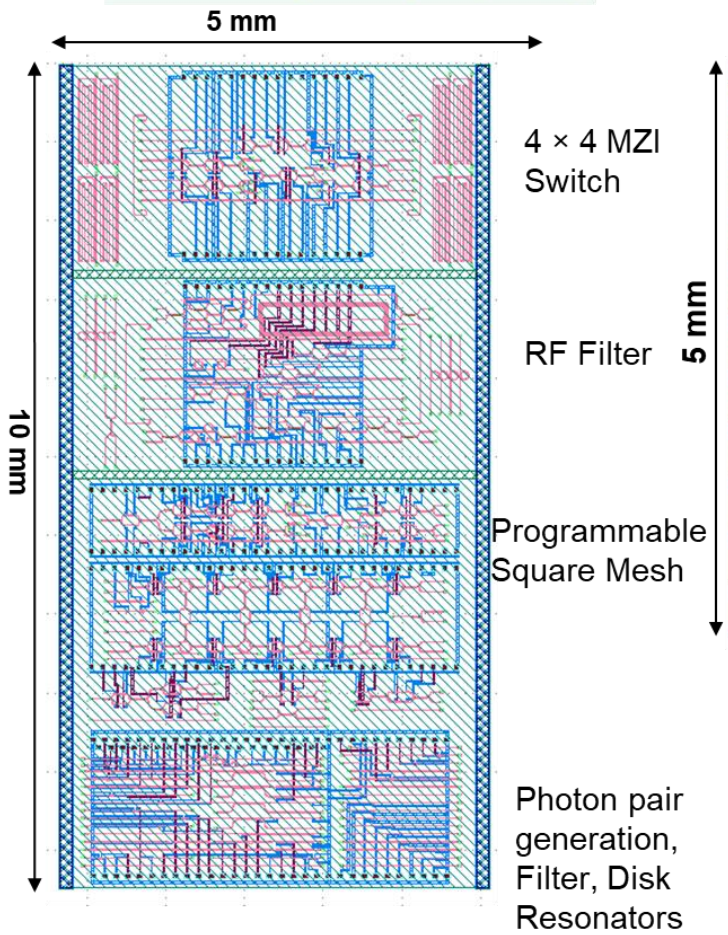


CPPICS : Quantum Efforts

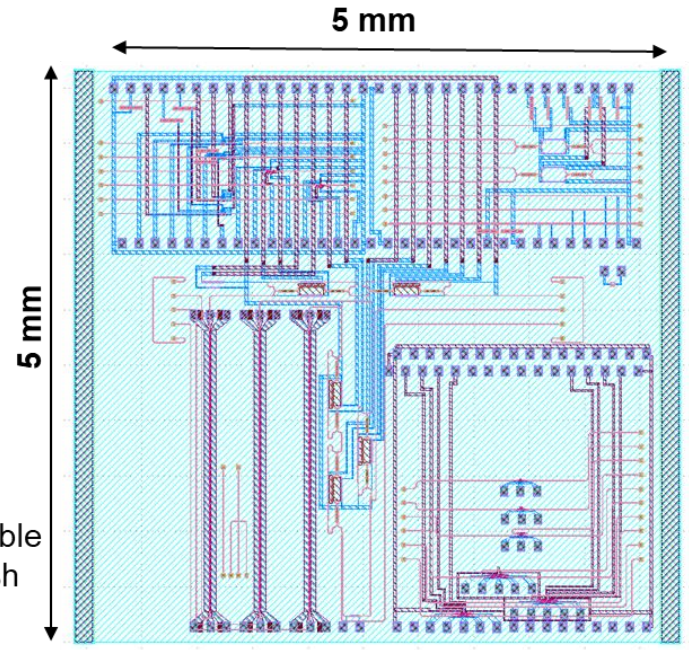
Tapeout Design Layout for Fabrication at IMEC Belgium

Faculty Collaborator: Anil Prabhakar, Janakiraman Viraraghavan, Saurabh Saxena and Sudharsanan Srinivasan

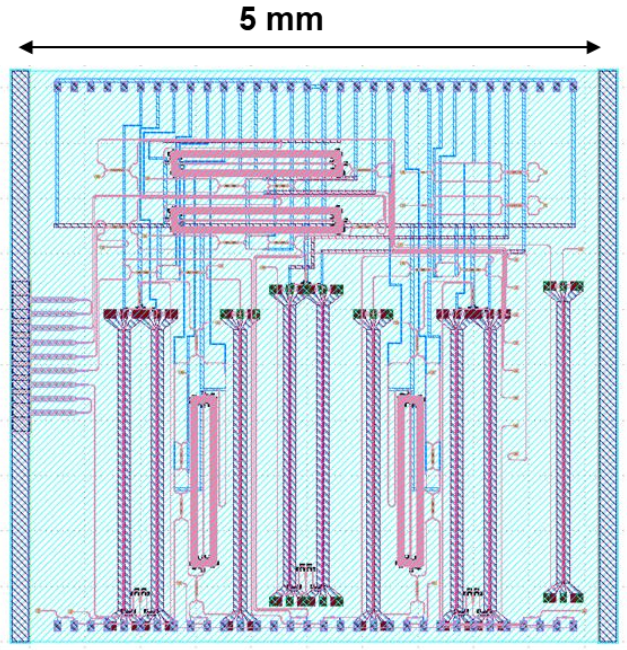
Passive Tape Out (Jun, 2022)



Active Tape Out (Oct, 2022)



RF filter, Modulators, Switches, Photon Pair Source



Quantum Key Distribution Chip

Expected delivery date of fabricated chips: June/July 2023

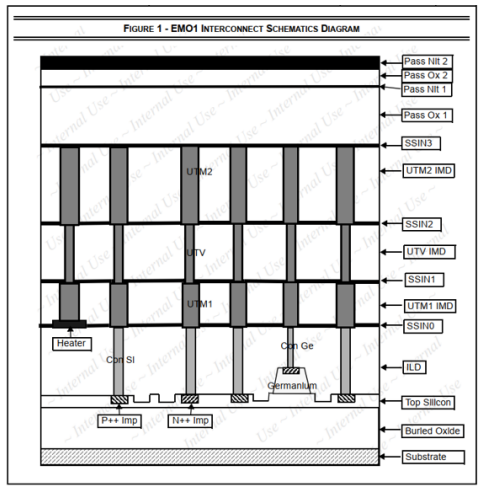
CPPICS : Quantum Efforts

Industry Collaboration: R & D Partnership with SilTerra Silicon Photonics Foundry Malaysia

Faculty Collaborators: Anjan Chakravorty, Deleep Nair, and Janakiraman Viraraghavan

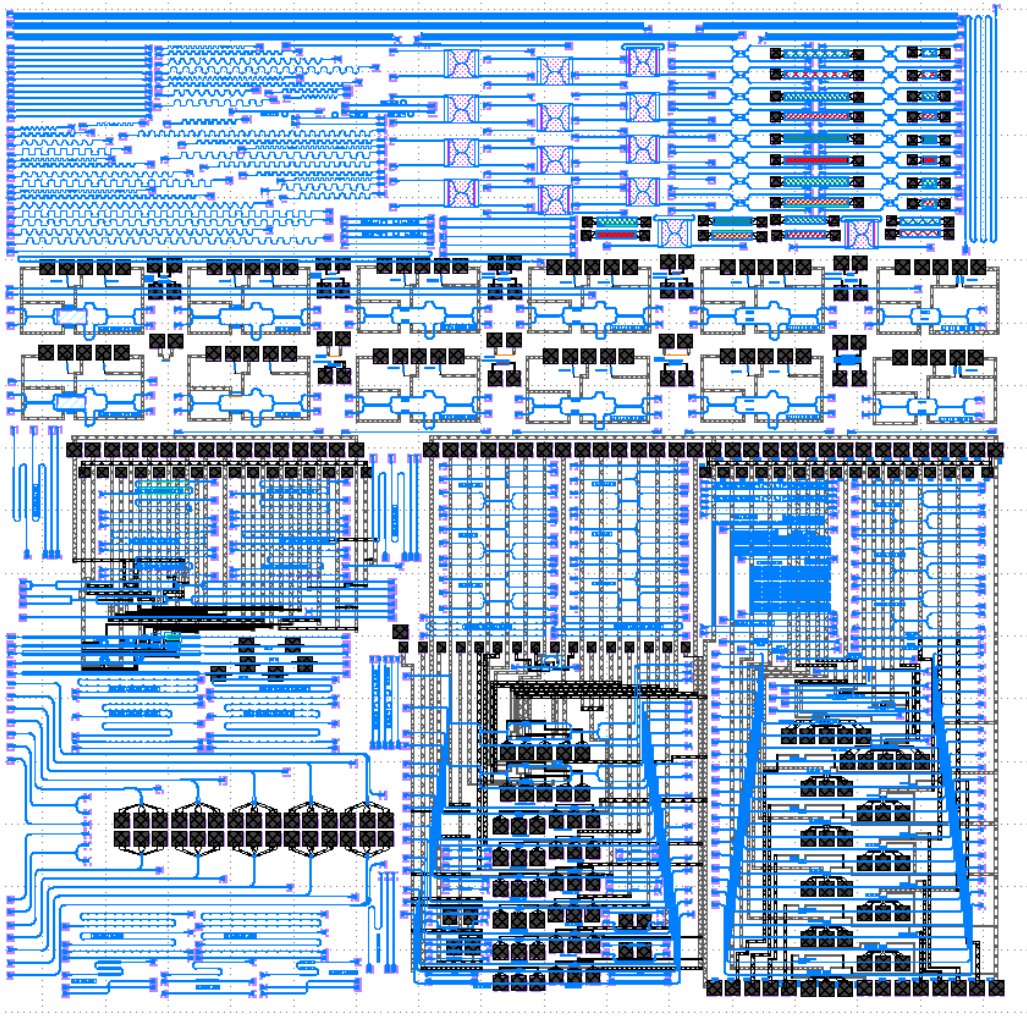
Design layout comprised of > 100 test structures submitted for internal tapeout for PDK development through compact modelings

SILTERRA



List of Important Test Structures:

- Singlemode & Multimode Waveguides
- Waveguide Crossings
- Grating Couplers
- Directional Couplers
- Mach-Zehnder Interferometers
- Delay Line Interferometers
- Thermo-optic Phase Shifters
- Doped Resistors & Rectifier Diodes
- Various Reconfigurable Filter Structures
- Higher order optical filters
- Microring/Microdisk/DBR Modulators
- Si/Ge Photodetectors

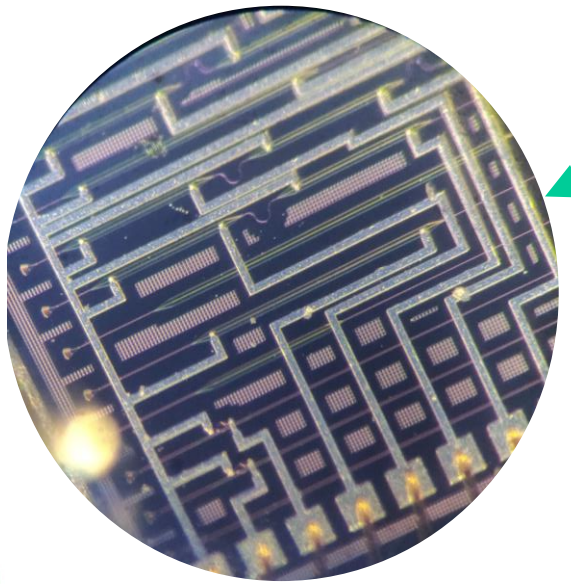


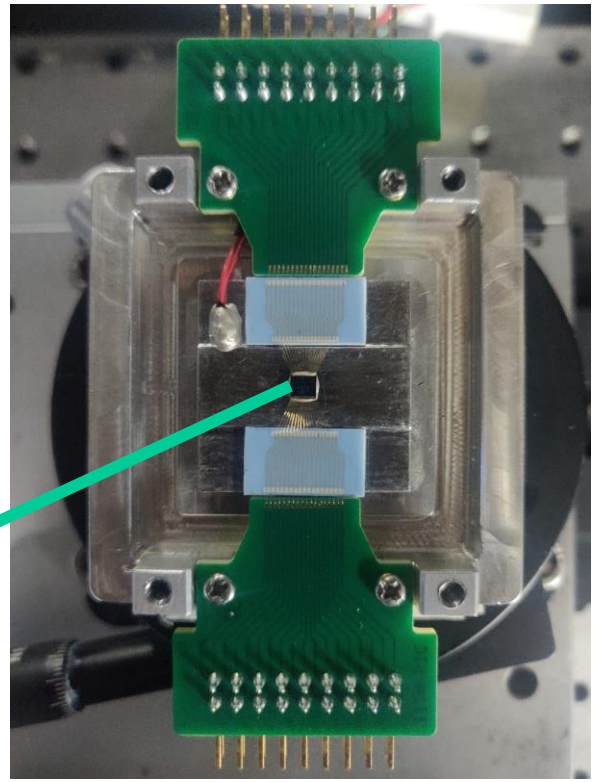
CPPICS : Quantum Efforts

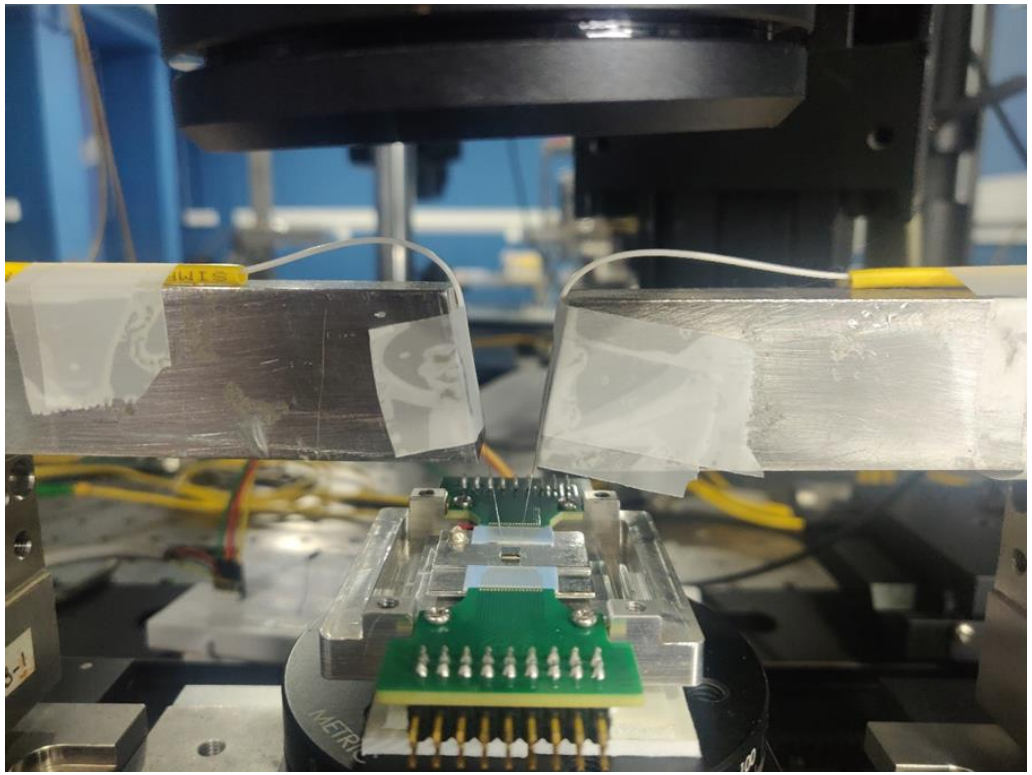
Industry Collaboration: Design Rule Development for PICS Packaging with Si2 Microsystems Bangalore

Faculty Collaborators: Deepa Venkitesh, Sudharsanan Srinivasan & Si2 Microsystems Team

Thermal Stabilization of System-in-Package Photonics Chip: 2nd Level Iteration







Thermo-optic evaluation qualified with DC power supply and i/o fiber-optic interfacings

Thank You